

CLAIMS

What is claimed is:

1. A processing element array, comprising:  
a logical array of processing elements logically arranged in a rectangular grid of logical rows and logical columns in which each processing element lies in only one logical row and one logical column, the processing elements in the array being divided into four sub-arrays each including the processing elements in a respective quartile of the logical array, the processing elements in each of the sub-arrays being physically positioned in a folded arrangement in which the processing elements in different logical rows are physically interleaved with each other and the processing elements in different logical columns are physically interleaved with each other; and  
a system of conductors coupling the processing elements in each of the logical rows and columns to each other.
2. The processing element array of claim 1 wherein the processing elements in each logical column are separated from each other by one processing element.
3. The processing element array of claim 1 wherein the processing elements in each logical row are separated from each other by three processing elements.
4. The processing element array of claim 1 wherein each of the sub-arrays comprises 256 processing elements.

5. The processing element array of claim 1 wherein the logical array of processing elements comprises a logical upper edge and a logical lower edge, and wherein the processing elements in each of the sub-arrays are physically positioned so that the processing elements adjacent the logical upper edge are physically positioned adjacent the processing elements adjacent the logical lower edge.

6. The processing element array of claim 1 wherein the logical array is divided into logical upper and lower sections of processing elements separated from each other by a divide line, and wherein the processing elements in each of the sub-arrays are physically positioned so that the lowest processing elements in the logical upper section are adjacent the highest processing elements in the logical lower section on opposite sides of the divide line.

7. The processing element array of claim 1 wherein each sub-array is logically divided into logical upper and lower sections of processing elements, and wherein the processing elements in each of the sub-arrays are physically positioned so that the processing elements in the logical upper section are interleaved with the processing elements in the logical lower section.

8. The processing element array of claim 1, further comprising a plurality of row registers logically positioned along one edge of the logical array at the end of respective logical rows and a plurality of column registers logically positioned along an adjacent edge of the logical array at the end of respective logical columns.

9. The processing element array of claim 8 wherein the logical array of processing elements comprises a logical upper edge and a logical lower edge, and wherein the column registers are physically positioned so that they are physically

adjacent the processing elements that are adjacent the logical upper edge and the logical lower edge of the logical array.

10. The processing element array of claim 9 wherein the column registers are physically positioned adjacent one physical edge of each sub-array.

11. The processing element array of claim 8 wherein the logical array of processing elements comprises a logical left edge and a logical right edge, and wherein the row registers are physically positioned so that they are physically adjacent the processing elements that are adjacent the logical left edge and the logical right edge of the logical array.

12. The processing element array of claim 11 wherein the row registers are physically positioned at the middle of each sub-array.

13. An integrated circuit active memory device comprising:  
a memory device having a data bus containing a plurality of data bus bits;

a logical array of processing elements each of which is coupled to a respective group of the data bus bits, each of the processing elements having an instruction input coupled to receive processing element instructions for controlling the operation of the processing elements, the processing elements in the array being logically arranged in a rectangular grid of logical rows and logical columns in which each processing element lies in only one logical row and one logical column, the processing elements in the array being divided into four sub-arrays each including the processing elements in a respective quartile of the logical array, the processing elements in each of the sub-arrays being physically positioned in a folded arrangement in which the processing elements in different logical rows are physically interleaved with each

other and the processing elements in different logical columns are physically interleaved with each other;

a system of conductors coupling the processing elements in each of the logical rows and columns to each other;

an array control unit being operable to generate a sequence of array control unit instructions responsive to each of a plurality of array control unit commands applied to a command input of the array control unit;

a memory device control unit coupled to the memory device, the memory device control unit being operable to generate and to couple respective sets of memory commands to the memory device responsive to each of a plurality of memory device control unit commands applied to a command input of the memory device control unit; and

a command engine coupled to the array control unit and the memory device control unit, the command engine being operable to couple to the array control unit respective sets of the array control unit commands and to couple to the memory device control unit respective sets of the memory device control unit commands responsive to respective task commands applied to a task command input of the command engine.

14. The active memory device of claim 13 wherein the memory device comprises a dynamic random access memory device.

15. The active memory device of claim 13 wherein the processing elements in each logical column are separated from each other by one processing element.

16. The active memory device of claim 13 wherein the processing elements in each logical row are separated from each other by three processing elements.

17. The active memory device of claim 13 wherein each of the sub-arrays comprises 256 processing elements.

18. The active memory device of claim 13 wherein the logical array of processing elements comprises a logical upper edge and a logical lower edge, and wherein the processing elements in each of the sub-arrays are physically positioned so that the processing elements adjacent the logical upper edge are physically positioned adjacent the processing elements adjacent the logical lower edge.

19. The active memory device of claim 13 wherein the logical array is divided into logical upper and lower sections of processing elements separated from each other by a divide line, and wherein the processing elements in each of the sub-arrays are physically positioned so that the lowest processing elements in the logical upper section are adjacent the highest processing elements in the logical lower section on opposite sides of the divide line.

20. The active memory device of claim 13 wherein each sub-array is logically divided into logical upper and lower sections of processing elements, and wherein the processing elements in each of the sub-arrays are physically positioned so that the processing elements in the logical upper section are interleaved with the processing elements in the logical lower section.

21. The active memory device of claim 13, further comprising a plurality of row registers logically positioned along one edge of the logical array at the

end of respective logical rows and a plurality of column registers logically positioned along an adjacent edge of the logical array at the end of respective logical columns.

22. The active memory device of claim 21 wherein the logical array of processing elements comprises a logical upper edge and a logical lower edge, and wherein the column registers are physically positioned so that they are physically adjacent the processing elements that are adjacent the logical upper edge and the logical lower edge of the logical array.

23. The active memory device of claim 22 wherein the column registers are physically positioned adjacent one physical edge of each sub-array.

24. The active memory device of claim 21 wherein the logical array of processing elements comprises a logical left edge and a logical right edge, and wherein the row registers are physically positioned so that they are physically adjacent the processing elements that are adjacent the logical left edge and the logical right edge of the logical array.

25. The active memory device of claim 24 wherein the row registers are physically positioned at the middle of each sub-array.

26. A computer system, comprising:  
a host processor having a processor bus;  
at least one input device coupled to the host processor through the processor bus;  
at least one output device coupled to the host processor through the processor bus;

at least one data storage device coupled to the host processor through the processor bus; and

an active memory device, comprising:

a memory device having a data bus containing a plurality of data bus bits;

a logical array of processing elements each of which is coupled to a respective group of the data bus bits, each of the processing elements having an instruction input coupled to receive processing element instructions for controlling the operation of the processing elements, the processing elements in the array being logically arranged in a rectangular grid of logical rows and logical columns in which each processing element lies in only one logical row and one logical column, the processing elements in the array being divided into four sub-arrays each including the processing elements in a respective quartile of the logical array, the processing elements in each of the sub-arrays being physically positioned in a folded arrangement in which the processing elements in different logical rows are physically interleaved with each other and the processing elements in different logical columns are physically interleaved with each other;

a system of conductors coupling the processing elements in each of the logical rows and columns to each other;

an array control unit being operable to generate a sequence of array control unit instructions responsive to each of a plurality of array control unit commands applied to a command input of the array control unit;

a memory device control unit coupled to the memory device, the memory device control unit being operable to generate and to couple respective sets of memory commands to the memory device responsive to each of a plurality of memory device control unit commands applied to a command input of the memory device control unit; and

a command engine coupled to the array control unit and the memory device control unit, the command engine being operable to couple to the array control unit respective sets of the array control unit commands and to couple to the memory device control unit respective sets of the memory device control unit commands responsive to respective task commands received from the host processor.

27. The active memory device of claim 26 wherein the memory device comprises a dynamic random access memory device.

28. The active memory device of claim 26 wherein the processing elements in each logical column are separated from each other by one processing element.

29. The active memory device of claim 26 wherein the processing elements in each logical row are separated from each other by three processing elements.

30. The active memory device of claim 26 wherein each of the sub-arrays comprises 256 processing elements.

31. The active memory device of claim 26 wherein the logical array of processing elements comprises a logical upper edge and a logical lower edge, and wherein the processing elements in each of the sub-arrays are physically positioned so that the processing elements adjacent the logical upper edge are physically positioned adjacent the processing elements adjacent the logical lower edge.



32. The active memory device of claim 26 wherein the logical array is divided into logical upper and lower sections of processing elements separated from each other by a divide line, and wherein the processing elements in each of the sub-arrays are physically positioned so that the lowest processing elements in the logical upper section are adjacent the highest processing elements in the logical lower section on opposite sides of the divide line.

33. The active memory device of claim 26 wherein each sub-array is logically divided into logical upper and lower sections of processing elements, and wherein the processing elements in each of the sub-arrays are physically positioned so that the processing elements in the logical upper section are interleaved with the processing elements in the logical lower section.

34. The active memory device of claim 26, further comprising a plurality of row registers logically positioned along one edge of the logical array at the end of respective logical rows and a plurality of column registers logically positioned along an adjacent edge of the logical array at the end of respective logical columns.

35. The active memory device of claim 34 wherein the logical array of processing elements comprises a logical upper edge and a logical lower edge, and wherein the column registers are physically positioned so that they are physically adjacent the processing elements that are adjacent the logical upper edge and the logical lower edge of the logical array.

36. The active memory device of claim 35 wherein the column registers are physically positioned adjacent one physical edge of each sub-array.

37. The active memory device of claim 34 wherein the logical array of processing elements comprises a logical left edge and a logical right edge, and wherein the row registers are physically positioned so that they are physically adjacent the processing elements that are adjacent the logical left edge and the logical right edge of the logical array.

38. The active memory device of claim 37 wherein the row registers are physically positioned at the middle of each sub-array.

39. A method of coupling a plurality of processing elements to each other, the processing elements being logically arranged in a rectangular array of logical rows and logical columns that is divided into four logical sub-arrays each of which includes the processing elements in a respective quartile of the logical array, the method comprising:

fabricating the processing elements in respective locations so that the processing elements in different logical rows are physically interleaved with each other and the processing elements in different logical columns are physically interleaved with each other; and

coupling the processing elements in each of the logical rows and columns to each other.

40. The method of claim 39 wherein the act of fabricating the processing elements in respective locations so that the processing elements in different logical columns are physically interleaved with each other comprises physically interleaving the processing elements in each logical column so that they are separated from each other by one processing element.

41. The method of claim 39 wherein the act of fabricating the processing elements in respective locations so that the processing elements in different logical rows are physically interleaved with each other comprises physically interleaving the processing elements in each logical row so that they are separated from each other by three processing elements.

42. The method of claim 39 wherein the logical array of processing elements comprises a logical upper edge and a logical lower edge, and wherein the act of fabricating the processing elements in respective locations so that the processing elements in different logical rows are physically interleaved with each other and the processing elements in different logical columns are physically interleaved with each other comprises fabricating the processing elements so that the processing elements adjacent the logical upper edge are physically positioned adjacent the processing elements adjacent the logical lower edge.

43. A method of coupling a plurality of processing elements to each other, the processing elements being logically arranged in a rectangular array of logical rows and logical columns, the method comprising:

logically dividing the logical array in half to form two logical sub-arrays;  
logically folding each of the logical sub-arrays; and  
logically positioning the logical sub-arrays adjacent each other.

44. The method of claim 43 wherein the act of logically folding each of the logical sub-arrays comprises:

dividing each of the logical sub-arrays in equal halves separated from each other by a dividing line; and

logically folding each of the logical sub-arrays so that a portion of each logical sub-array is logically folded with a logical edge of the logical sub-array adjacent the dividing line.

45. The method of claim 44 wherein the act of logically positioning the logical sub-arrays adjacent each other comprises logically positioning the sub-arrays so that the folded portions of the sub-arrays face toward each other with the logical edges adjacent each other.